CL-451 Product Family Specification

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USING THIS DOCUMENT

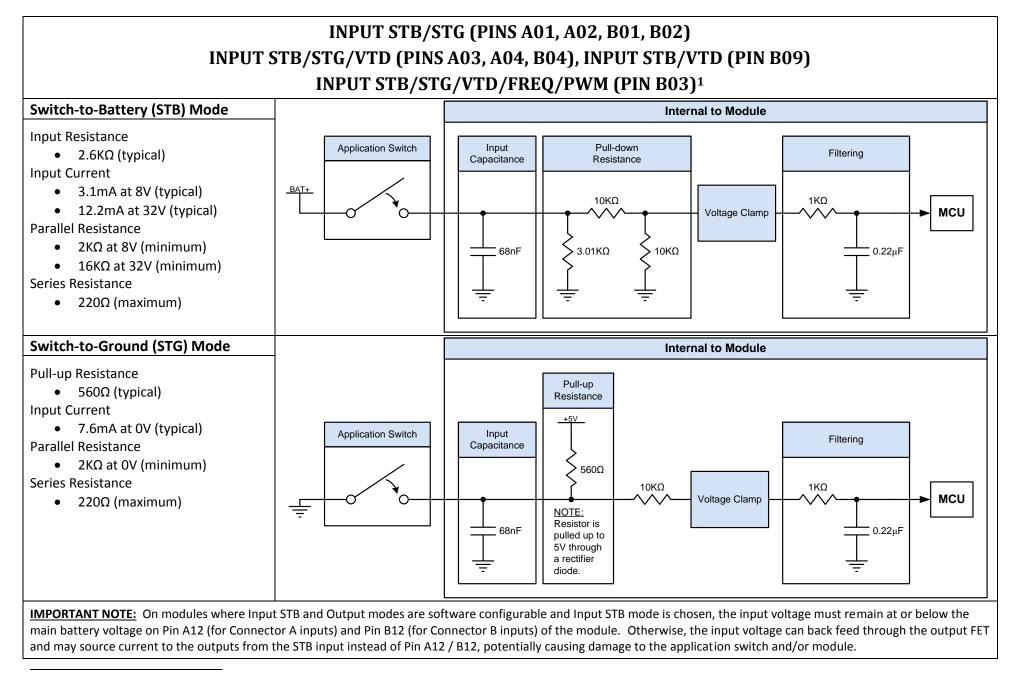
The specifications contained herein represent all possible configurations for this product family. The actual configurations available on each module may be a subset of this specification. Please refer to the module-specific datasheet for the connector pinout and configurations that are available.

USER LIABILITY

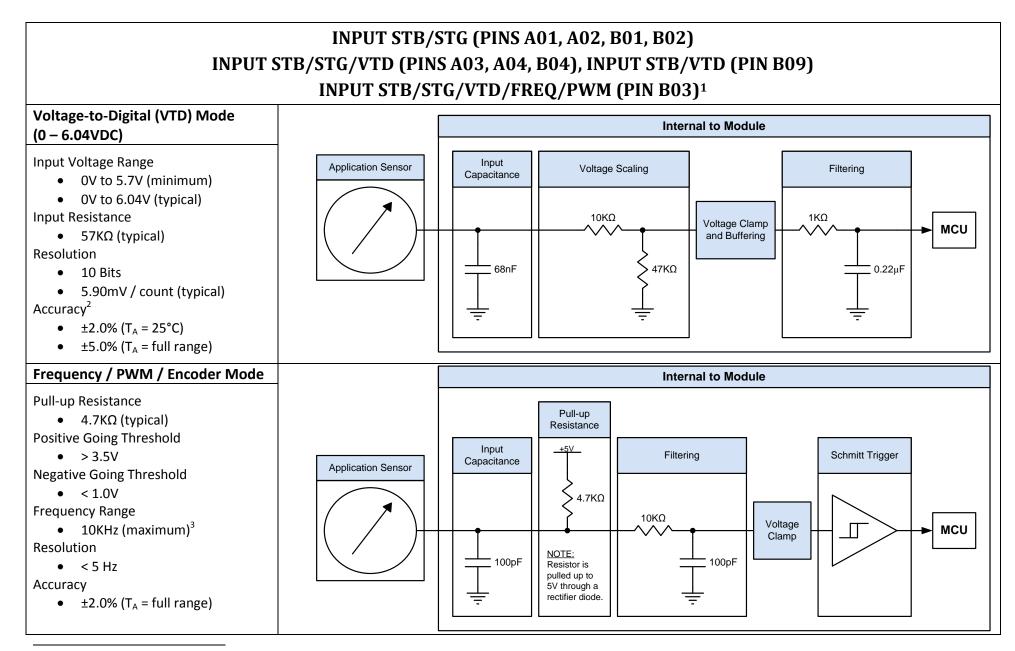
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The products described herein, including without limitation, product features, specifications, designs, availability and pricing, are subject to change by HED[®] at any time without notice.



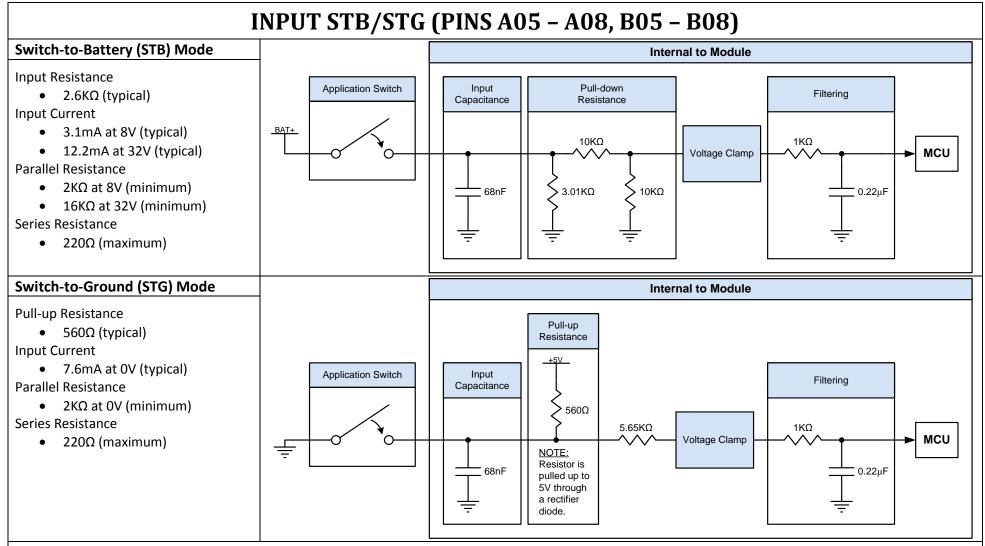
¹ Pin B03 has an input capacitance of 100pF.



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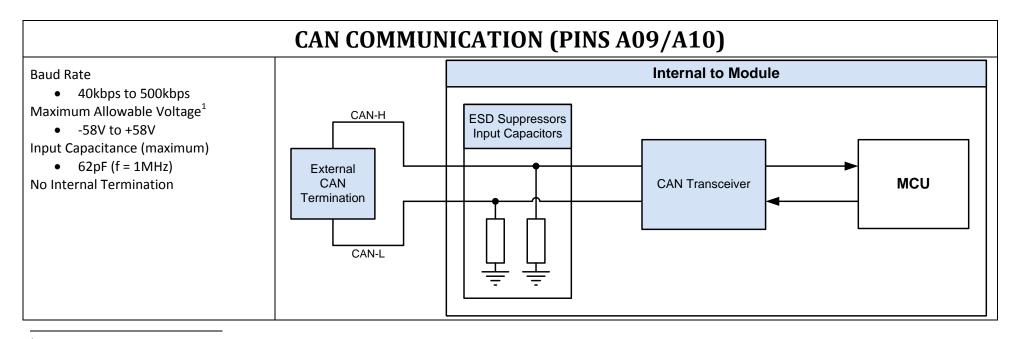
² VTD accuracy is estimated using datasheet maximums and a weighted average of worst-case and root-sum-square (RSS) methods. It is considered as a percentage of the full-scale input voltage range.

³ Frequency range maximum assumes square wave, open-drain, sinking sensor at 50% duty cycle.

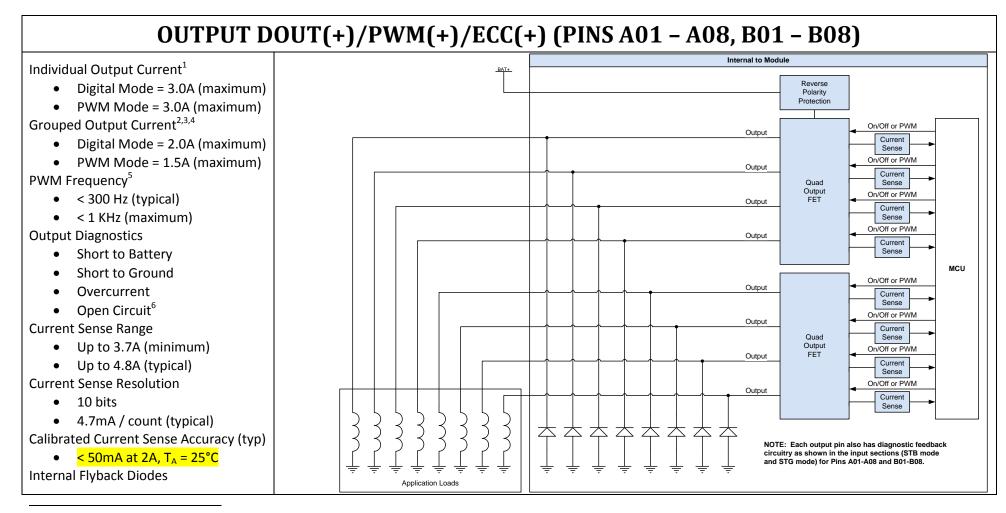


IMPORTANT NOTES:

- On modules where Input STB and Output modes are software configurable and Input STB mode is chosen, the input voltage must remain at or below the main battery voltage on Pin A12 (for Connector A inputs) and Pin B12 (for Connector B inputs) of the module. Otherwise, the input voltage can back feed through the output FET and may source current to the outputs from the STB input instead of Pin A12 / B12, potentially causing damage to the application switch and/or module.
- 2) Pins A05-A08 and B05-B08 can be software configured as outputs, STB inputs, or STG inputs; however, all pins must have the same I/O type chosen. These pins must either be selected as all 8 outputs, all 8 STB inputs, or all 8 STG inputs.



¹ Maximum allowable voltage defines the voltage extremes that the transceiver can tolerate. Exposure to these voltages for extended periods may affect device reliability.



¹ Individual Output Current specifies the maximum current for an individual output channel. Additional restrictions regarding total output current, number of active channels, etc. will apply and are specified in the Grouped Output Current parameter. PWM outputs assume 250Hz frequency.

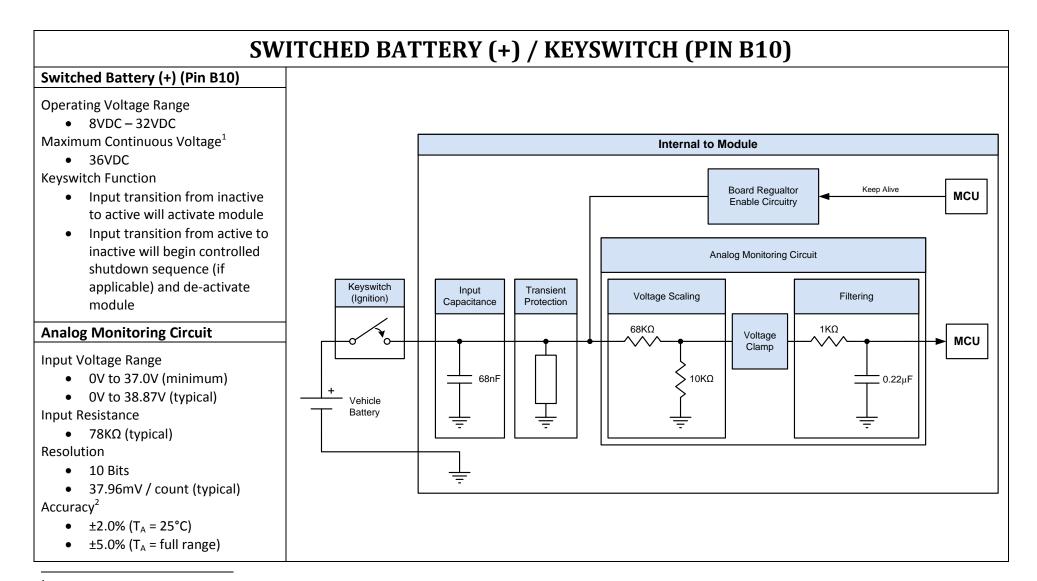
⁵ The output driver is best suited for PWM frequencies of 300 Hz or less. PWM frequencies of up to 1 KHz are possible, but at reduced output current and duty cycle range.

⁶ Open circuit can be detected when the output is active using current sense feedback for load currents of at least 250mA and duty cycle of 100%. Open circuit can be detected when the output is inactive using the pull-up resistor for loads that are not influenced by the associated pull-up current (see Input STG mode circuit diagram and parameters).

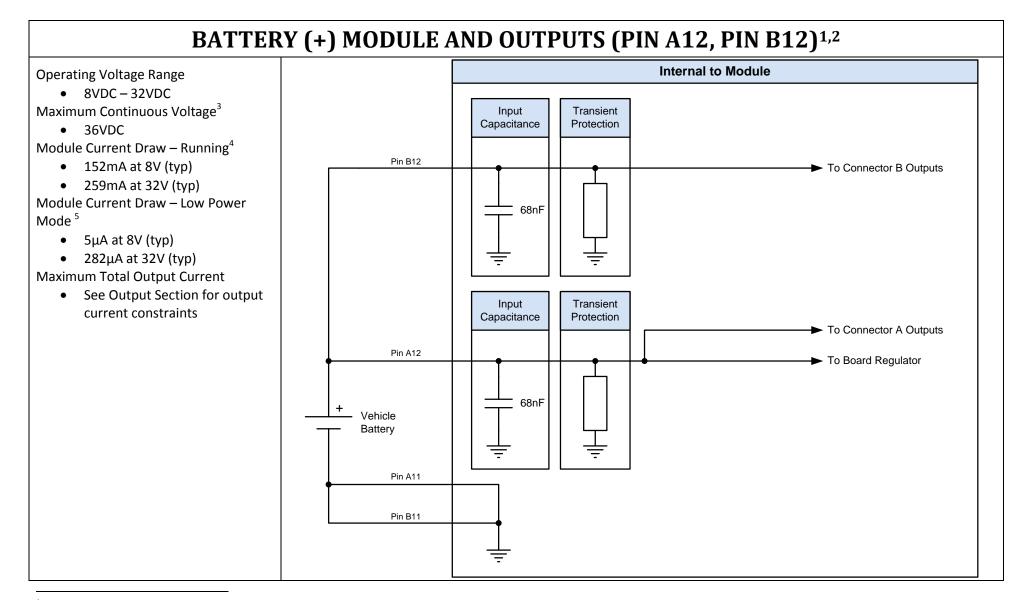
² Output current is constrained in groups of four pins (quad output FET). Pin groups are A01-A04, A05-A08, B01-B04, and B05-B08. It is strongly recommended to level the total output current across each of the groups as much as possible for best thermal performance.

³ Output current maximums assume all four channels in the group are active simultaneously and the module is at maximum ambient temperature. PWM outputs assume 250Hz frequency. Output current may be increased per channel (up to the individual output current maximum) if not all channels are active simultaneously or other channels are at a reduced load current. Please contact HED[®] for further information.

⁴ Maximum total output current for Pins A01-A08 is 10 Amps. Maximum total output current for Pins B01-B08 is 10 Amps.



¹ Exposure to maximum voltages for extended periods may affect device reliability.



¹ Pin A12 provides power to module and Connector A outputs. Pin B12 provides power to Connector B outputs only.

² Pins A11 and B11 must be connected at a single point to Battery (-).

³ Exposure to maximum voltages for extended periods may affect device reliability.

⁴ Module current draw is measured with I/O inactive, no CAN communication, and keyswitch (Pin B10) active.

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REVISION HISTORY			
Revision	Date	EC #	Changes
A1	7/23/14	314-307	Initial Release. Items in yellow identify general market design targets requiring specific board configuration or firmware feature support to complete remaining verification testing.